

**IN THE CLAIMS**

Please amend the claims as follows:

Claim 1 (currently amended): A switch circuit formed on a semiconductor substrate, comprising:

    a first terminal to which a signal of transmission object is inputted;  
    a second terminal from which a signal of transmission object is outputted;  
    a first transistor formed in a first semiconductor region in said semiconductor substrate, which has one of [[a]] source and [[a]] drain terminals connected to said first terminal and another thereof connected to said second terminal;  
    a control circuit ~~which controls~~ configured to control a gate voltage of said first transistor; and  
    a first rectifying element which has an anode terminal connected to said first terminal, a cathode terminal connected to a power supply terminal of said control circuit, said first rectifying element being formed in a second semiconductor region in said semiconductor substrate separate from said first semiconductor region.

Claim 2 (original): The switch circuit according to claim 1, wherein said first transistor is a p type.

Claim 3 (currently amended): The switch circuit according to claim 1, further comprising:

    a [[third]] second rectifying element which has an anode terminal to which a power supply voltage is supplied, and a cathode terminal connected to the power supply terminal of

said control circuit, said [[third]] second rectifying element being formed [[on]] in a semiconductor region separate from said first semiconductor region.

Claim 4 (currently amended): The switch circuit according to claim 3, wherein said third rectifying element is formed on said second semiconductor region includes the semiconductor region in which said second rectifying element is formed.

Claim 5 (currently amended): The switch circuit according to claim 1, further comprising:

a second transistor of a conductive type different from that of said first transistor which has one of a source terminal and a drain terminal connected to said first terminal and another thereof connected to said second terminal, said second transistor turning on/off in sync with said first transistor.

Claim 6 (original): The switch circuit according to claim 5, wherein said second transistor is formed in a third semiconductor region separate from said first and second semiconductor regions.

Claim 7 (currently amended): The switch circuit according to claim 1, wherein said first and second terminals are bi-directional input/output terminals, and further comprising:  
a ~~fourth~~ second rectifying element formed in said second semiconductor region, which has an anode terminal connected to said second terminal and a cathode terminal connected to [[a]] the power supply terminal of said control circuit.

Claim 8 (currently amended): The switch circuit according to claim 1, further comprising:

a [[fifth]] second rectifying element which has an anode terminal connected to [[a]] the source terminal of said first transistor, and a cathode terminal connected to a substrate of said first transistor; and

a [[sixth]] third rectifying element which has an anode terminal connected to [[a]] the drain terminal of said first transistor, and a cathode terminal connected to the substrate of said first transistor; and

~~a back gate of said second transistor which is grounded.~~

Claim 9 (original): The switch circuit according to claim 1, wherein said first rectifying element is formed of an MOS transistor which has a source or drain terminal shortcut to a gate terminal.

Claim 10 (currently amended): The switch circuit according to claim [[2]] 7, wherein said at least one of said first and second rectifying elements is formed of an MOS transistor which has a source or a drain terminal shortcut to a gate terminal.

Claim 11 (currently amended): The switch circuit according to claim [[3]] 5, wherein said control circuit includes:

a first logic circuit ~~which controls a~~ configured to control the gate voltage of said first transistor; and

a second logic circuit ~~which controls~~ configured to control a gate voltage of said second transistor by a signal inverting an output of said first logic circuit;

~~a cathode terminal of said third rectifying element being connected to a power supply terminal of said first logic circuit and a power supply terminal of said second logic circuit.~~

Claim 12 (currently amended): A switch circuit formed on a semiconductor substrate, comprising:

    a first terminal to which a signal of transmission object is inputted;  
    a second terminal from which a signal of transmission object is outputted;  
    a p-type first transistor which has one of [[a]] source and [[a]] drain terminals connected to said first terminal and another thereof connected to said second terminal;  
    a control circuit ~~which controls~~ configured to control a gate voltage of said first transistor;  
    a first rectifying element formed in a first semiconductor region in said semiconductor substrate, which has an anode terminal to which a first power supply voltage is supplied and a cathode terminal connected to a back gate of said first transistor; and  
    a second rectifying element formed in a second semiconductor region in said semiconductor substrate separate from said first semiconductor region, which has an anode terminal connected to said first terminal and a cathode terminal connected to a power supply terminal of said control circuit.

Claim 13 (currently amended): The switch circuit according to claim 12, further comprising:

    a third rectifying element formed in a semiconductor region separate from said first semiconductor region, which has an anode terminal to which [[the]] a second power supply voltage is supplied and a cathode terminal connected to [[a]] the power supply terminal of said control circuit.

Claim 14 (currently amended): The switch circuit according to claim 13, wherein ~~said third rectifying element is formed in said second semiconductor region~~ includes the semiconductor region in which said third rectifying element is formed.

Claim 15 (original): The switch circuit according to claim 12, further comprising a second transistor of a conductive type different from that of said first transistor, which has one of a source terminal and a drain terminal connected to said first terminal, and another thereof connected to said second terminal, said second transistor turning on/off in sync with said first transistor.

Claim 16 (original): The switch circuit according to claim 15, wherein said second transistor is formed in a third semiconductor region separate from said first and second semiconductor regions.

Claim 17 (currently amended): The switch circuit according to claim 12, wherein said first and second terminals are bi-directional input/output terminals, and further comprising: a ~~fourth~~ third rectifying element formed in said second semiconductor region which has an anode terminal connected to said second terminal and a cathode terminal connected to [[a]] the power supply terminal of said control circuit.

Claim 18 (currently amended): The switch circuit according to claim 12, further comprising:

a [[fifth]] third rectifying element which has an anode terminal connected to the source terminal of said first transistor, and a cathode terminal connected to the substrate back gate of said first transistor; and

a [[sixth]] fourth rectifying element which has an anode terminal connected to the drain terminal of said first transistor, and a cathode terminal connected to the substrate back gate of said first transistor; and

~~a back gate of said second transistor which is grounded.~~

Claim 19 (currently amended): The switch circuit according to claim [[13]] 15, wherein said control circuit includes:

a first logic circuit ~~which controls~~ configured to control the gate voltage of said first transistor; and

a second logic circuit ~~which controls~~ configured to control a gate voltage of said second transistor by a signal inverting an output of said first logic circuit;

~~wherein a cathode terminal of said third rectifying element is connected to power supply terminals of said first and second logic circuits.~~

Claim 20 (currently amended): A switch circuit formed on a semiconductor substrate, comprising:

a first terminal to which a signal of transmission object is inputted;

a second terminal from which a signal of transmission object is outputted;

a first transistor formed in a first semiconductor region in said semiconductor substrate, which has one of [[an]] emitter and [[a]] collector terminals connected to said first terminal and another thereof connected to said second terminal;

a control circuit ~~which controls~~ configured to control a base voltage of said first transistor; and

a first rectifying element which has an anode terminal connected to said first terminal, a cathode terminal connected to a power supply terminal of said control circuit, said first

rectifying element being formed in a second semiconductor region in said semiconductor substrate separate from said first semiconductor region.

Claim 21 (currently amended): A switch circuit formed on a semiconductor substrate, comprising:

    a first terminal to which a signal of transmission object is inputted;  
    a second terminal from which a signal of transmission object is outputted;  
    a p-type first transistor which has one of [[an]] emitter and [[a]] collector terminals connected to said first terminal and another thereof connected to said second terminal;  
    a control circuit ~~which controls~~ configured to control a base voltage of said first transistor;  
    a first rectifying element formed in a first semiconductor region in said semiconductor substrate, which has an anode terminal to which a power supply voltage is supplied and a cathode terminal connected to a back base of said first transistor; and  
    a second rectifying element formed in a second semiconductor region in said semiconductor substrate separate from said first semiconductor region, which has an anode terminal connected to said first terminal and a cathode terminal connected to a power supply terminal of said control circuit.